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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/698,622	10/27/2000	Jyh-Ming Jong	P4928/06145.003001	4922

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EXAMINER	
BAYARD, EMMANUEL	
ART UNIT	**PAPER NUMBER**
2638	

DATE MAILED: 01/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/698,622	JONG ET AL.	
	Examiner	Art Unit	
	Emmanuel Bayard	2638	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 October 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7 and 9-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7 and 9-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This is in response to amendment filed on 10 /14/05 in which claims 1-7 and 9-13 are pending. The applicant's amendments have been fully considered but they are moot based on the new ground of rejection.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-6, 9 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Morzano U.S. Patent No 6,791,370 B1 in view of Ogiwara U.S. Patent No 5,729,208.

As per claims 1 and 9, Morzano discloses an apparatus for detecting a noise error of a signal comprising: a voltage input buffer is the same as the claimed (high comparator) (see fig.1 element 11 and col.1, lines 15-27 and col.2, lines 1-7 and col.4, lines 23-67 and col.6, lines 27-29) that references a high voltage limit with the signal and generates an output; a voltage input buffer is the same as the claimed (low comparator) (see fig.1 element 10 and col.1, lines 15-27 and col.2, lines 1-7 and col.4, lines 23-67 and col.6, lines 27-29) that references a low voltage limit with the signal and generates an output; and a circuit (see fig.1 element 12) that processes the high comparator output and the low comparator output, wherein both the high comparator

output and at least one of low comparator output directly clock (see fig.1 elements 106-107 and col.5, lines 26-30) the circuit.

However Morzano does not teach wherein the circuit generates an alarm if a noise error is detected.

Ogiwara teach detection circuit that detects a breakage is the same as the claimed (noise error is detected) and generate a fault (see abstract and col.1, lines 25-40 and col.2, lines 11-30).

It would have been obvious to one of ordinary skill in the art to implement the teaching of Ogiwara into Morzano as to generate from the captured logic states of the first and second comparison outputs indicative of an open circuit condition and accurately detect faulty condition as taught by Ogiwara (see abstract and col2, lines 25-29).

As per claim 2, the apparatus of Morzano includes a high-to-low sub-circuit that rising) signal transition and a low-to-high sub-circuit during a (0)(falling) signal transition (see col.2, lines 1-7 and col.6, lines 1-20). Furthermore implementing such teaching into Ogiwara to detect noise error would have been obvious to one skilled in the art as to generate from the captured logic states of the first and second comparison outputs indicative of an open circuit condition and accurately detect faulty condition as taught by Ogiwara (see abstract and col.2, lines 25-29).

As per claims 3, 11-12 Ogiwara teaches a plurality of flip-flop circuits (see fig.3 element 40, 42) and Mux is functionally equivalent to the claimed (XOR logic gate) (see fig.3 element 44). Furthermore implementing such teaching into the delay buffer (see

fig.1 element 10 or 11) of Morzano would have been obvious to one skilled in the art as to generate from the captured logic states of the first and second comparison outputs indicative of an open circuit condition and accurately detect faulty condition as taught by Ogiwara (see abstract and col.2, lines 25-29).

As per claim 4, the apparatus of Morzano does include differential amplifier (see fig.2 element 25 and col.4, lines 43-45).

As per claim 5, the apparatus of Morzano does include differential amplifier (see fig.2 element 25 and col.4, lines 43-45), which is known in the art as differential sense amplifier.

As per claims 6 and 10, the apparatus of Morzano includes high voltage limit and the low voltage limit (see col.1, lines 14-15). Furthermore generating a 30 mV voltage into Morzano and Ogiwara to detect noise error would have been obvious to one skilled in the art as to generate from the captured logic states of the first and second comparison outputs indicative of an open circuit condition and accurately detect faulty condition as taught by Ogiwara (see abstract and col.2, lines 25-29).

As per claims 7 and 13, Morzano teaches discloses an apparatus for detecting a noise error of a signal comprising: a voltage input buffer is the same as the claimed (high comparator) (see fig.1 element 11 and col.1, lines 15-27 and col.2, lines 1-7 and col.4, lines 23-67 and col.6, lines 27-29) that references a high voltage limit with the signal and generates an output; a voltage input buffer is the same as the claimed (low comparator) (see fig.1 element 10 and col.1, lines 15-27 and col.2, lines 1-7 and col.4, lines 23-67 and col.6, lines 27-29) that references a low voltage limit with the signal and

generates an output, wherein the difference between the high voltage limit and the low voltage limit is 30 mV; and a high and low circuit (see fig.1 element 12) and a low-to-high sub-circuit that detects falling and rising signal transitions (see col.2, lines 1-7 and col.6., lines 1-20) comprises a delay buffer (see figs.1, 7 elements 14 or 15, 72 and col4, lines 29-35 and col.7,lines 35-60).

However Morzano does not teach detects a noise error during a falling signal transition that detects a noise error during a rising and falling signals transition wherein the sub-circuit generates an alarm if a fault is the same as the claimed (noise error is detected) wherein at least one of the high to-low sub-circuit and the low-to-high sub-circuit generates an alarm if a noise error is detected comprises a plurality of flip-flop circuits (see fig.3 element 40, 42) and Mux is functionally equivalent to the claimed (XOR logic gate) (see fig.3 element 44).

Ogiwara teach detection circuit that detects a breakage is the same as the claimed (noise error is detected) and generate a fault (see abstract and col.1, lines 25-40 and col.2, lines 11-30) which functionally equivalent to the claimed detects a noise error during a falling signal transition that detects a noise error during a rising and falling signals transition wherein the sub-circuit generates an alarm if a fault is the same as the claimed (noise error is detected) wherein at least one of the high to-low sub-circuit and the low-to-high sub-circuit generates an alarm if a noise error is detected (see abstract and col.1, lines 25-40 and col.2, lines 11-30) comprising a plurality of flip-flop circuits (see fig.3 element 40, 42) and Mux is functionally equivalent to the claimed (XOR logic gate) (see fig.3 element 44).

It would have been obvious to one of ordinary skill in the art to implement the teaching of Ogiwara into Morzano as to generate from the captured logic states of the first and second comparison outputs indicative of an open circuit condition and accurately detect faulty condition as taught by Ogiwara (see abstract and col2, lines 25-29).

Conclusion

3. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Maddux et al U.S. Patent No 6,421,801 B1 teaches a testing IO timing.

Betti et al U.S. Patent No 5,623,220 teaches an offset reduction.

Matsuda U.S. 6,084,607 teaches an ink type.

Bizzan U.S Patent no 6,154,548 teaches an audio mute.

Walker U.S. Patent No 5,825,431 teaches an H-sync to pixel.

Ishimo et al U.S. Patent No 6,194,933 B1 teaches an input circuit for phase lag.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Emmanuel Bayard whose telephone number is 571 272 3016. The examiner can normally be reached on Monday-Friday (7:Am-4:30PM) Alternate Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Vanderpuye Kenneth can be reached on 571 272 3078. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Emmanuel Bayard
Primary Examiner
Art Unit 2638

12/31/05

EMMANUEL BAYARD
PRIMARY EXAMINER